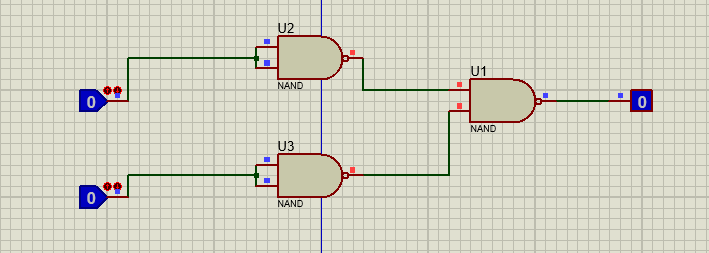
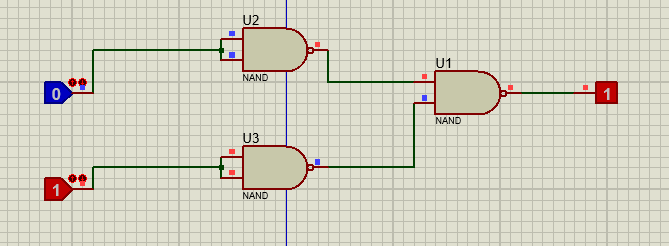
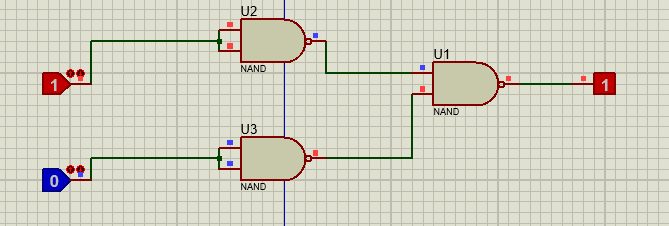
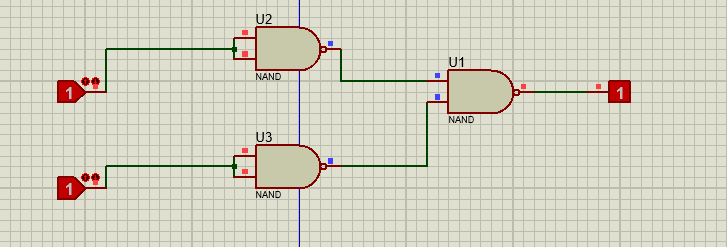
NAND gate as an OR gate :

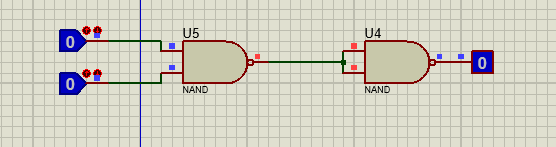


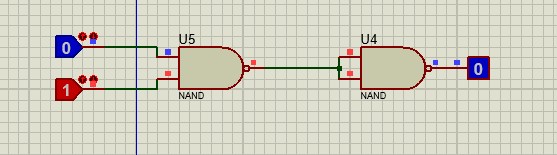


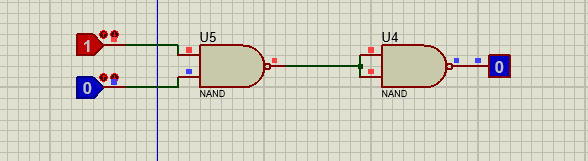


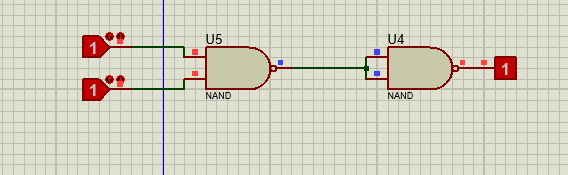


NAND gate as an AND gate :

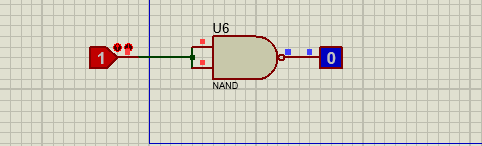


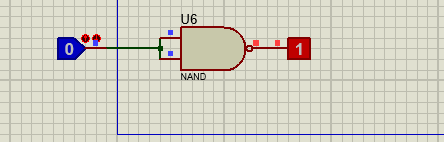




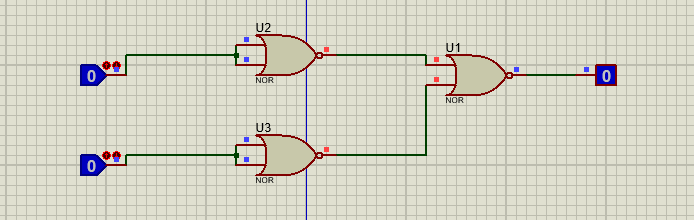


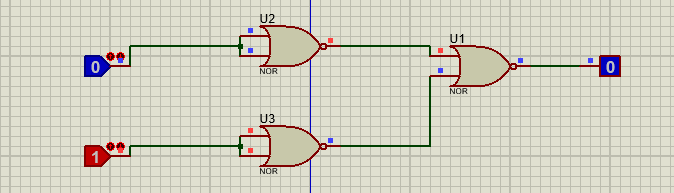
NAND gate as a NOT gate :

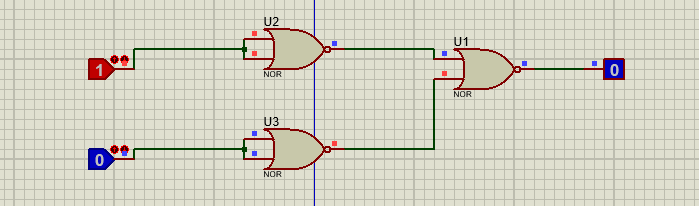


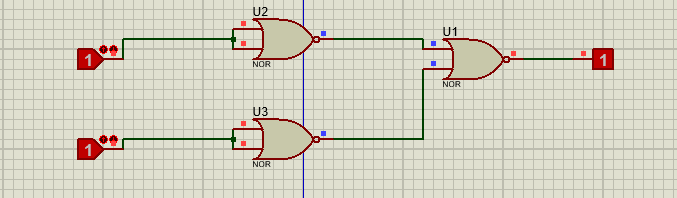


NOR gate as an AND gate :

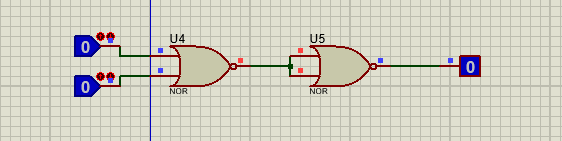


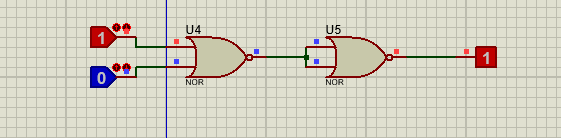


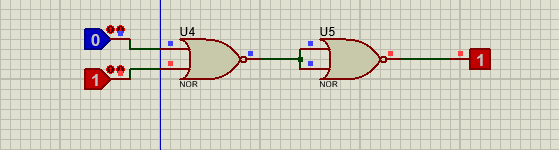


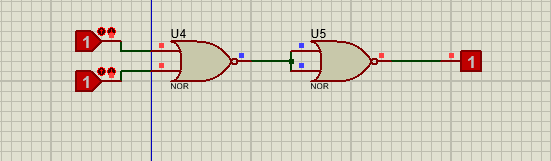


NOR gate as an OR gate :









NOR gate as a NOT gate :

